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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/045,237 | 10/23/2001 | Jong-Sun Kim | 8021-67 (SS-15860-US) | 9923 |

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| EXAMINER | |
|---|---|
| NGUYEN, HAI L | |
| **ART UNIT** | **PAPER NUMBER** |
| 2816 | |

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/045,237 | KIM, JONG-SUN | |
| | Examiner | Art Unit | |
| | Hai L. Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-17,21-23,26 and 27* is/are rejected.

7)☒ Claim(s) *10,11,18,19,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04 March 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 14-17 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art, Fig. 1 in the present application.

With respect to claim 14, the admitted prior art in Fig. 1 shows a delay locked loop (DLL) comprising a basic clock generator (103); a first mixer (104, 105a, 105b, 105c) for generating a first clock signal (CLK0) in response to the plurality of basic clock signals; a second mixer (104, 105a) for generating a second clock signal (CLK90) which is 90 degrees out-of-phase with the first clock signal in response to the plurality basic clock signals; a clock buffer (108) for generating a first internal clock signal (TCLK) in response to the first clock signal and a second internal clock signal (TCLK90) in response to the second clock signal; a phase detector (112); and a digital-to-analog converter (113) for controlling phase ranges of the first and second clock signals generated in first and second mixers in response to an output of the phase detector.

With regard to claims 15-17, the references also meet the recited limitations in these claims (as disclosed in the specification page 2, line 8 through page 2, line 13 and shown in Fig. 1).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-9, 12, 20-23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Fig. 1 in the present application, in view of Sumita et al. (US 5,764,091).

With respect to claim 5, the admitted prior art in Fig. 1 shows a delay locked loop (DLL) comprising a first amplifier (101) for receiving an external clock signal (EXT_CLK); a first duty corrector (102); a basic clock generator (103); a mixer (104); a second amplifier (106); a third amplifier (107); a clock buffer (108); a third duty corrector (110) for correcting the duty of the second internal clock signal (TCLK90) and feeding an output of the third duty corrector back to the third amplifier; an output replica (111); a phase detector (112) for comparing and detecting phases of the external clock signal and the second internal clock signal; and a digital-to-analog converter (113) for controlling phase ranges of the first and second clock signals generated in the mixer in response to an output of the phase detector. Fig. 1 of the admitted prior art meets all the claimed limitations, except for a second duty corrector (210' in instant Fig. 2) for correcting the duty of the first internal clock signal (TCLK). Sumita et al. teaches in Fig. 1 a semiconductor integrated circuit having a duty corrector circuit (10) for each of the plurality of internal clocks wherein each of the internal clocks associated with a circuit block (51a –51d). Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention

was made to utilize that teaching of Sumita et al. in Fig. 1 of the prior art by implementing a duty corrector (as same as duty corrector 110) for correcting a duty of the first internal clock signal for the advantage being able to provide a duty ratio-guaranteed of the first internal clock signal.

Claim 1 is similarly rejected; note the above discussion with regard to claim 5.

With regard to claims 2-4, 6-9, and 12, the references also meet the recited limitations in these claims (as disclosed in the specification page 2, line 8 through page 2, line 13 and shown in Fig. 1).

Claim 20 is similarly rejected; note the above discussion with regard to claims 5 and 14.

With regard to claims 21-23 and 26, the references also meet the recited limitations in these claims (as disclosed in the specification page 2, line 8 through page 2, line 13 and shown in Fig. 1).

5. Claims 13 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Fig. 1 in the present application, in view of Sumita et al., as applied to claims 5, 6, 9, and 20 above, and further in view of Allen et al. (US 5,911,063).

The above discussed circuit of the prior art meets all of the claimed limitations except for the limitation that the clock buffer (108 in instant Fig. 1) has a path having a chain of serially connected inverters (108a & 108b) for each of the plurality of clock signals. Allen et al. teaches in Fig. 1B a clock buffer circuit (16) having a chain of serially connected inverters (16B, 16C) for each of the plurality of clock signals which is provided to a plurality of receiving elements. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize a chain of serially connected inverters for each of the plurality of clock signals, which is provided to a plurality of receiving elements, with the prior art (Fig. 3 of

Redman-White et al.) in order to minimizes the effect of clock skew of the clock signals received at each of the plurality of elements.

### *Allowable Subject Matter*

6. Claims 10, 11, 18, 19, 24, and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest each of the first and second mixers (404 & 405 in instant Fig. 6) comprising a selector (503) for generating select signals in response to an output of an the digital-to-analog converter (414); a first phase MUX (501) for selecting phase ranges of the plurality of basic clock signals in response to the select signals and determining the phase range of the plurality of basic clock signals as the phase ranges of the first clock signal (CLK0, CLK0B); and a second phase MUX (502) for selecting the phase ranges of the plurality of basic clock signals in response to the select signals and determining the phase ranges of the plurality of basic clock signals as the phase ranges of the second clock signal (CLK90, CLK90B) configured in a delay locked loop (400 in instant Fig. 5) comprises a basic clock generator (403); a clock buffer (408); a phase detector (413); a digital-to-analog converter (414); and a specific structural limitations such as a first mixer (404) and a second mixer (405).

### *Conclusion*

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Kim (US 6,452,432) is cited as of interest because it discloses a Signal

processing circuits having a pair of delay locked loop (DLL) circuits for adjusting a duty-cycle of a periodic digital signal and methods of operating same.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN
September 7, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800